

As stated in MPEP §§ 2142-2143.01, to establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. Obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either explicitly or implicitly in the references themselves or in the knowledge generally available to one of ordinary skill in the art. "The test for an implicit showing is what the combined teachings, knowledge of one of ordinary skill in the art, and the nature of the problem to be solved as a whole would have suggested to those of ordinary skill in the art." In re Kotzab, 217 F.3d 1365, 1370, 55 USPQ2d 1313, 1317 (Fed. Cir. 2000). See also In re Fine, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988); In re Jones, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992).

The prior art, either alone or in combination, does not teach or suggest all the features of the independent claims. The present invention relates to a method for manufacturing a semiconductor device and a heat treatment method. Specifically, the method comprises forming a semiconductor layer over a glass substrate; forming an insulating layer over the semiconductor layer; forming an island-like light-absorbing layer over the semiconductor layer with the insulating layer interposed therebetween; performing a heat treatment for the semiconductor layer and the insulating layer by selectively heating the light-absorbing layer through an irradiation of the pulsed light; and patterning the light-absorbing layer after performing the heat treatment. For the reasons provided below, Dairiki and Joo, either alone or in combination, do not teach or suggest the above-referenced features of the present invention.

The Official Action asserts that "Dairiki discloses a method for manufacturing a semiconductor device (See Figs. 4, 10A-10C, 11A-11C, and Cols. 1-28) comprising: forming a semiconductor layer 202 over a glass substrate 201, forming an island-like insulating layer 203 over the semiconductor layer, forming an island-like light-absorbing layer 205/206 over the semiconductor layer 202 with the insulating layer 203/204 interposed therebetween, the island-like light-absorbing layer being capable of absorbing a pulsed light, performing a heat treatment for the semiconductor layer and the insulating layer by selectively heating the light-absorbing layer through an irradiation of the pulsed light" (page 3, Paper No. 20060206). The Official Action concedes that "Dairiki fails to disclose the step of patterning the light-absorbing layer after performing the heat treatment" (*Id.*). The Office Action asserts that "Joo discloses the method for manufacturing a semiconductor device similar to Dairiki's method and further discloses the step of patterning the light-absorbing layer (Fig. 4G; paragraph 0042) after performing the heat treatment (by light irradiation, paragraph 0041)" (*Id.*).

In the present invention, heat generated in the island-like light-absorbing layer by the irradiation of the pulsed light uniformly heats a portion where the semiconductor layer is formed whereas the other portions are less heated. This concept of the present invention is not suggested in Joo (for example, Figure 4F) and in Dairiki.

Further, even if Dairiki's process is combined with Joo's process, the present invention as claimed in claims 1-14 and 16-23 is not obtained.

Since Dairiki and Joo do not teach or suggest all the claim limitations, a *prima facie* case of obviousness cannot be maintained. Accordingly, reconsideration and withdrawal of the rejections under 35 U.S.C. § 103(a) are in order and respectfully requested.

Should the Examiner believe that anything further would be desirable to place this application in better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number listed below.

Respectfully submitted,



Eric J. Robinson
Reg. No. 38,285

Robinson Intellectual Property Law Office, P.C.
PMB 955
21010 Southbank Street
Potomac Falls, Virginia 20165
(571) 434-6789